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10/743,113	12/22/2003	Kyung Yun Jung	SUN-DA-114T	8491

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
3663	

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12/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,113	JUNG, KYUNG YUN	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination ('RCE') under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/25/07 has been entered.

Response to Amendment

Amendment filed with said RCE on 9/25/07 forms the basis for this Office Action. In said Amendment applicant added new claims 4-10. Comments on Remarks submitted with said Amendment are included below in "Response to Arguments".

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the anti-fuse must be clearly identified in terms of its constituent part(s) through numerals and arrows in a comprehensive manner and as such must be shown or the feature anti-fuse canceled from the claims. Arrow with reference numeral 108c, referring to "anti-fuse" does not point specifically to any single region or combination of regions in Figures 4 and 5D. No new matter should be entered. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures

appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. The Specification is objected to for not uniquely identifying the claimed anti-fuse. In particular, the "anti-fuse" is identified by an arrow and reference numeral 108c, but the reference numeral points to a poly-interpretable object, either the insulating layer an upper conductive portion of an anti-fuse, or to what is generally understood to be an anti-fuse, namely: conductive layer/insulating layer/conductive layer. See, e.g., Gerstner (ISBN 978-0-85296-961-8), especially page 318, for the definition of anti-fuse as two

conducting layer separated by an insulating layer. (N.B.: Gerstner is cited not for teaching, but instead for establishing accepted nomenclature). Especially in conjunction with recent comment in Remarks, filed 9/25/07 and in an After-Final communication, applicant appears to confine the anti-fuse to only either the insulating layer or the insulating layer and conducting layer opposite the conductive material of a plug.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Because "anti-fuse" is not uniquely defined in the Specification, as explained above, the anti-fuse of the claimed invention is indefinite because it is poly-interpretable and hence indefinite, containing either only the insulating layer between two conductive layers, or said insulating layers with either one or two of said conductive layers abutting said insulating layer.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. ***Claims 1-10*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. The reason for this rejection is the same as the reason provided for the objection to the Specification under sections 2 and 3 above.

9. ***Claims 6 and 10*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. In particular, nowhere n the Specification as originally filed does applicant recite that the third contact plug is narrower than the second contact plug.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. ***Claims 1-10*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The reason for this rejection is the same as the reason provided for the objection to the Specification under sections 4 and 5 above.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. ***Claims 1 and 3*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tung et al (5,248,632) in view of either Man (5,533,635) (previously cited) and Wei et al (5,923,075) (rejection according to 'first interpretation' as defined below), or in view of

Mann (5,533,635) (previously cited) alone (rejection according to 'second interpretation' as defined below).

N.B.: The rejection is provided subject to the noted indefiniteness under 35 U.S.C. 112, second paragraph, wherein examiner distinguishes two interpretations covered separately in the rejection, i.e., the interpretation of anti-fuse as merely the insulating layer, henceforth referred to as the 'first interpretation'; or the anti-fuse as defined by Gertsner, which examiner holds as common nomenclature as understood by those of ordinary skill in the art, henceforth referred to as the 'second interpretation'.

According to the first interpretation, Tung et al teach (Figure 4, also Figure 9) a semiconductor device (col. 1, l. 5-8 and col. 3, l, 11-20), comprising:

a capacitor having a bottom electrode (MOS transistor channel including drain 20: see col. 3, l. 11-20 and realizing that a MOS transistor is also a MOS capacitor (see, e.g., S. Wolf, "Silicon Processing for the VLSI Era", Volume 3 – "The submicron MOSFET", pages 83-85) (previously made of record), a dielectric layer 16 formed on the bottom electrode (col. 3, l. 30), and an upper electrode 18 (loc.cit.) formed on the dielectric layer, the capacitor being formed on a semiconductor substrate (12, 14 or 12/14: col. 3, l. 22-39);

a first insulating layer 22 (col. 3, l. 32-33) formed on the semiconductor substrate to cover the capacitor;

a plurality of first contact plugs (28 (col. 3, l. 41) and another not shown in the Figures)(col. 3, l. 35-39) (N.B.: see Fig. 10 and discussion: note that a plurality of devices as depicted in either Figure 4 or Figure 9 are integrated (col. 1, l. 5-9) formed in

a plurality of first via holes of the first insulating layer, each of the plurality of said first contact plugs being electrically connected to either the bottom electrode or the upper electrode, namely the bottom electrode through drain 20(col. 3, l. 35-39));

a first metal wiring formed on the insulating layer and connected to the bottom electrode through one of the first contact plugs is inherent given the "contact regions 24 are formed *through* the thick oxide layer to provide contact to"... "the diffused regions" col. 3, l. 35-39), because in order for contact regions 24 (Figure 1) are thereby admitted to have an electrical connection to a conductive material positioned *on* said insulating layer;

a second insulating layer 30 (col. 3, l. 55-59 and Figure 4) or 48 (col. 5, l. 20-21 and Figure 9) formed on the first insulating layer;

a second contact plug 34 or 46 (Figures 4 and 9, resp.: see col. 3, l. 60 – col. 4, l. 3, and col. 5, l. 5-17) in the second insulating layer formed on the first insulating layer and connected to the upper electrode 18 through another one of the first contact plugs(namely: 28 taking into account the conductive nature of TiW layer 26 (col. 3, l. 47-48));

an anti-fuse 36 (col. 3, l. 60 – col. 4, l. 15: Figure 4) or anti-fuse 50 (Figure 9 and col. 5, l. 30-46) formed on the second contact plug 34 or 46 (Figures 4, 9 resp.) not necessarily in a second via hole of the second insulating layer (30 or 48 do not necessarily contain said anti-fuse thus interpreted), but electrically connected to the second contact plug (loc.cit.).; and

a third contact plug 40a or 54a (col. 4, l. 16-27 and col. 5, l. 18-29) not necessarily filling a second via hole; and

a second metal wiring 60 formed on the second insulating layer (connecting to 40 must be on said second insulating layer 30 or 48: see Figures 4 and 9) (col. 5, l. 47-61 with Figure 10).

Tung et al do not necessarily teach the limitation "third contact plug does not directly contact the second insulating layer", nor does Tung necessarily teach the limitation that said anti-fuse is formed in a second contact hole as claimed.

However, it would have been obvious to include said limitation ad (a) in view of Man, who, in a patent on a MOS transistor (col. 2, l. 56 – col. 3, l. 35 and Figure 3) with Al comprising interconnect (see title, abstract and col. 2, l. 62-63), hence analogous art, teach the interposing of a TiW barrier metal layer 34 (col. 2, l. 61-62) between said interconnect 36 and the underlying dielectric layer 24 col. 2, l. 61).

Motivation to include the teaching of the interposition of a TiW metal barrier layer between dielectric layer 30 and Al-comprising metal layer 40a derives at least from the presence of Al also in the third contact plug by Tung et al (see col. 4, l. 19-27 in Tung et al), implying the desirability to keep the Al in 36 away from the dielectric material of 24, and the suggestion by Tung et al themselves to also include TiW in the material embodiment of element 40. It would have been particularly obvious, in light of this suggestion by Tung et al, to include the teaching by Man in the form of a barrier layer of TiW separating a third contact plug comprising Al and dielectric 30 (i.e., the claimed second insulating layer) from the underlying "second insulating layer" 30. Note that all that is needed from Man is a modification in the teaching by Tung et al so as to teach a third contact plug comprising an aluminum copper compound separated from 30 by a

TiW barrier layer, rather than the teaching by Tung et al "an aluminum copper compound and TiW".

Combination of the teaching by Man with the invention by Tung et al immediately meets limitation (a) through re-definition of the third contact plug as the aluminum copper compound portion of element 40a.

Furthermore, it would have been obvious to include limitation (b) above, in view of Wei et al, who, in a patent on an anti-fuse cell (title and abstract), hence art analogous to Tung et al, teach the anti-fuse to be "covered by an insulating layer blanket deposited over all" (col. 3, l. 20+ and Figure 7), through which openings are etched for electrical contacts, including one contact plug 38 contacting the anti-fuse cell through 28 (Figure 7 and col. 3, l. 22+). In the combined invention, an insulating layer is blanket deposited over all in the device of Figures 4 or 9, said insulating layer abutting insulating layer 30 and hence together with insulating layer 30 interpretable as "second insulting layer", with a second via hole analogous to element 38 in Wei et al is etched and filled with the material occupying the latter, thus constructing a hole extendable to the claimed contact hole. Said anti-fuse cell with said contact plug in the final structure is interpretable as one contact hole and meets the limitations on second contact hole. *Motivation* to include the teaching by Wei et al immediately derives from the additional protection for which the device as depicted in Figures 4 and 9 is in dire need, considering the absence of any passivation offering protection to the exposed and non-level portions at the upper surface.

According to the second interpretation, Tung et al teach (Figure 4, also Figure 9) a semiconductor device (col. 1, l. 5-8 and col. 3, l, 11-20), comprising:

a capacitor having a bottom electrode (MOS transistor channel including drain 20: see col. 3, l. 11-20 and realizing that a MOS transistor is also a MOS capacitor (see, e.g., S. Wolf, "Silicon Processing for the VLSI Era", Volume 3 – "The submicron MOSFET", pages 83-85) (previously made of record), a dielectric layer 16 formed on the bottom electrode (col. 3, l. 30), and an upper electrode 18 (loc.cit.) formed on the dielectric layer, the capacitor being formed on a semiconductor substrate (12, 14 or 12/14: col. 3, l. 22-39);

a first insulating layer 22 (col. 3, l. 32-33) formed on the semiconductor substrate to cover the capacitor;

a plurality of first contact plugs (28 (col. 3, l. 41) and another not shown in the Figures)(col. 3, l. 35-39) (N.B.: see Fig. 10 and discussion: note that a plurality of devices as depicted in either Figure 4 or Figure 9 are integrated (col. 1, l. 5-9) formed in a plurality of first via holes of the first insulating layer, each of the plurality of said first contact plugs being electrically connected to either the bottom electrode or the upper electrode, namely the bottom electrode through drain 20(col. 3, l. 35-39));

a first metal wiring formed on the insulating layer and connected to the bottom electrode through one of the first contact plugs is inherent given the "contact regions 24 are formed *through* the thick oxide layer to provide contact to"... "the diffused regions" col. 3, l. 35-39), because in order for contact regions 24 (Figure 1) are thereby admitted

to have an electrical connection to a conductive material positioned *on* said insulating layer;

a second insulating layer 30 (col. 3, l. 55-59 and Figure 4) or 48 (col. 5, l. 20-21 and Figure 9) formed on the first insulating layer;

a second contact plug 34 or 46 (Figures 4 and 9, resp.: see col. 3, l. 60 – col. 4, l. 3, and col. 5, l. 5-17) in the second insulating layer formed on the first insulating layer and connected to the upper electrode 18 through another one of the first contact plugs(namely: 28 taking into account the conductive nature of TiW layer 26 (col. 3, l. 47-48));

an anti-fuse 42 with anti-fuse element 36 (col. 3, l. 60 – col. 4, l. 15: Figure 4) or anti-fuse 56 with anti-fuse element 50 (Figure 9 and col. 5, l. 30-46) formed on the second contact plug 34 or 46 (Figures 4, 9 resp.) in a second via hole of the second insulating layer (30 or 48) and electrically connected to the second contact plug (loc.cit.).; and

a third contact plug 40a or 54a (col. 4, l. 16-27 and col. 5, l. 18-29) filling the second via hole and formed within the anti-fuse (loc.cit.); and

a second metal wiring 60 formed on the second insulating layer (connecting to 40 must be on said second insulating layer 30 or 48: see Figures 4 and 9) (col. 5, l. 47-61 with Figure 10).

Tung et al do not necessarily teach the limitation "third contact plug does not directly contact the second insulating layer".

However, it would have been obvious to include said limitation in view of Man, who, in a patent on a MOS transistor (col. 2, l. 56 – col. 3, l. 35 and Figure 3) with Al

comprising interconnect (see title, abstract and col. 2, l. 62-63), hence analogous art, teach the interposing of a TiW barrier metal layer 34 (col. 2, l. 61-62) between said interconnect 36 and the underlying dielectric layer 24 col. 2, l. 61).

Motivation to include the teaching of the interposition of a TiW metal barrier layer between dielectric layer 30 and Al-comprising metal layer 40a derives at least from the presence of Al also in the third contact plug by Tung et al (see col. 4, l. 19-27 in Tung et al), implying the desirability to keep the Al in 36 away from the dielectric material of 24, and the suggestion by Tung et al themselves to also include TiW in the material embodiment of element 40. It would have been particularly obvious, in light of this suggestion by Tung et al, to include the teaching by Man in the form of a barrier layer of TiW separating a third contact plug comprising Al and dielectric 30 (i.e., the claimed second insulating layer) from the underlying "second insulating layer" 30. Note that all that is needed from Man is a modification in the teaching by Tung et al so as to teach a third contact plug comprising an aluminum copper compound separated from 30 by a TiW barrier layer, rather than the teaching by Tung et al "an aluminum copper compound and TiW".

Combination of the teaching by Man with the invention by Tung et al immediately meets limitation (a) through re-definition of the third contact plug as the aluminum copper compound portion of element 40a.

On claim 3: The device of claim 1 would necessarily have to be formed in order to function. Claim 3 fails to further limit the device of claim 1 other than simply form each of their components.

14. ***Claims 4, 5, 7 and 9*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tung et al (5,248,632) in view of Man (5,533,635) (previously cited) and Wei et al (5,923,075) (rejection according to 'first interpretation' as defined above).

As detailed, claims 1 and 3 are unpatentable over inter alia Tung et al in view of Man and Wei et al. Furthermore:

On claims 4 and 7: in the combined invention according to the first interpretation as defined above, the anti-fuse 36 or 50 according to the first interpretation is formed between the second contact plug 34 or 46 and the third contact plug (analogous to 38 in Wei et al) and between the second insulating layer 30 and the third contact plug (38 in Wei et al).

On claims 5 and 9: because in the combined invention according to the first interpretation the upper surface of the third contact (see element 38 in Wei et al) abuts the upper surface of the second insulating layer laterally (see element 36 in Wei et al) said upper surfaces are indeed in the same horizontal plane.

15. ***Claim 2*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Tung et al and Man as applied to claim 1 above, and further in view of Madan et al (6,141,240).

As detailed above, claim 1 is unpatentable over Tung et al in view of Man. Neither references necessarily teach the further limitation defined by claim 2.

However, it would have been obvious to include said further limitation in view of Madan et al, who, in a patent on a memory array, teach the bitline (i.e., drain) and wordline (i.e., gate) wirings to be perpendicular to each other (Figure 1 and col. 3, l. 38-

43). *Motivation* to include said teaching by Madan et al in the invention by Tung et al at least derives from the spatial efficiency achieved by the cubic arrangement.

16. ***Claims 6, 8 and 10*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tung et al, Man and Wei et al as applied to claims 1 and 3 above, and further in view of Kwok et al (5,903,042).

As detailed above, claims 1 and 3 are unpatentable over Tung et al in view of Man and Wei et al.

Neither Tung et al, nor Man nor Wei et al necessarily teach the further limitations on the relative width of the second and third contact plug nor on the lack of direct contact between third contact plug and insulating layer. However, it would have been obvious to include said limitations in view of Kwok et al, who, in a patent on an anti-fuse on a semiconductor body (col. 3, l. 30-40), hence art analogous to that of Tung et al, teach the anti-fuse dielectric 22 to align the edges of the third contact plug (col. 3, l. 60-64 and Figures 1) as a (first) embodiment among other variations of the fuse dielectric also including substantially planar fuse dielectrics (see element 122 in Kwok et al, Figure 12) as employed by Tung et al (Figure 9). The alignment of the edges prevents direct contact between third contact plug in 20 (Figure 1a) and second insulating layer 18 (col. 2, l. 57). Combining the teaching by Kwok et al, i.e., extending the analogous element 54 along the entire base of 54 and along its edges, meets the limitation and is motivated at least by the apparent equivalent design shown in Kwok et al side by side with the design of Figure 9 in Tung et al. Furthermore, Kwok et al also offer an

embodiment wherein the width of the third contact is less ('narrower') than that of the width of the second contact plug (base 16).

In conclusion, a device is found in the prior art that differs from the claimed device by the substitution of some components with other components, namely: device of Figure 9 by Tung et al is found differing in the extent and shape of the dielectric fuse 54. But other prior art (Kwok et al shows that the substituted components and their functions were known in the art (first embodiment by Kwok et al in known in the art). One of ordinary skill in the art could have substituted one known element for another and the results of the substitution would have been predictable, because all embodiments by Kwok et al are well-functioning anti-fuse devices. Therefore, the claim would have been obvious because the substitution of one known element (54 in Tung et al) for another (a fuse element of the form of element 22 of the first embodiment by Kwok et al) would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Response to Arguments

17. Applicant's arguments filed 9/25/07 have been fully considered but they are not persuasive. In particular, applicant's traverse that Tung et al fails to teach or suggest an anti-fuse in a second via hole and a third contact plug filling the second via hole depends on an unconventional interpretation of what is meant by anti-fuse, which, as witnessed for instance by Gerstner (ISBN 978-0-85296-961-8), is defined as consisting of two conducting layers separated by a thin dielectric layer". See page 318 in Gerstner. To expedite prosecution examiner herewith includes two rejection based on alternative

interpretations of anti-fuse, as explained in the references overhead, which are herewith included by reference in their entirety in response to applicant's arguments. Furthermore, with regard to the new claims, it is noted that the Specification as originally filed falls short of disclosing that the third contact plug is narrower than the second contact plug.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
December 9, 2007

Primary Examiner:

Johannes Mondt (Art Unit: 3663)